AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Previously presented) A method for generating program source code for translating high level code into instructions for a target processors, the method comprising:

determining a program code characteristic corresponding to said target processor;

deriving one or more program code modules in accordance with said desired program code characteristic; and

generating program source code for translating high level code into instructions for said target processor from said one or more program code modules.

2. (Previously presented) A method according to claim 1, for generating program source code for translating high level code into instructions for one of a plurality of target processors.

3. (Previously presented) A method according to claim 1, comprising forming agglomerated program source code from a plurality of program code modules in accordance with said desired program code characteristic.

4. (Original) A method according to claim 1, further comprising deriving said program code modules in accordance with a desired functionality for said target processor.

5. (Previously presented) A method according to claim 2~~1~~, wherein:

said step of determining comprises determining respective program code characteristics for respective ones of a plurality of target processors;

said step of deriving comprises deriving respective program code modules in accordance with said respective program code characteristics; and

said step of generating comprises generating program source code for translating high level code into instructions for said target processors from said program code modules.

6. (Original) A method according to claim 1, wherein said step of deriving comprises selecting one or more pre-defined program code modules in accordance with said program code characteristic from a plurality of available program code modules.

7. (Previously presented) A method according to claim 1, wherein said program code provides a virtual machine for said target processor.

8. (Previously presented) A method according to claim 1, wherein said program code comprises elements of a programming language.

9. (Previously presented) A method for creating program source code for translating between high level code and instructions for a target processor, comprising the steps of:

determining a program code characteristic corresponding to said target processor;

selecting one or more predefined program code modules in accordance with said program code characteristic; and

forming program source code for translating high level code into instructions for said target processor from said selected one or more predefined program code modules.

10. (Previously presented) A method according to claim 9, wherein said creating program source code for translating between high level code and instructions is for one of a plurality of target processors.

11. (Previously presented) A data processing apparatus for creating program source code for translating between high level code and instructions for a target processor, the data processing apparatus being configured to:

determine a program code characteristic corresponding to said target processor identifier input to said data processing apparatus;

derive one or more program code modules in accordance with said program code characteristic; and

create program source code for translating high level code into instructions for said target processor from said derived one or more program code modules.

12. (Previously presented) The data processing apparatus according to claim 11, further configured for creating program source code for translating between high level code and instructions for one of a plurality of target processors.

13. (Previously presented) An apparatus, comprising at least one program source code module of a plurality of program source code modules for translating between high level code and instructions for a target processor, said at least one program code module corresponding to a characteristic of said target processor and being selected from said plurality of program source code modules.

14. (Previously presented) The apparatus of claim 13, further comprising at least one additional program code modules for translating between high level code and instructions for respective ones of at least two target processors.

15. (Previously presented) The apparatus according to claim 14, wherein said at least two program code modules are selected from a plurality of predefined program code modules.

16. (Canceled)

17. (Canceled)

18. (Previously presented) The apparatus according to claim 13, wherein said program source code provides a virtual machine for said target processor.

19. (Previously presented) The apparatus according to claim 14, wherein said program source code provides a virtual machine for said target processor or processors.

20. (Previously presented) The apparatus according to claim 13, wherein said program source code comprises elements of a programming language.

21. (Previously presented) The apparatus according to claim 14, wherein said program source code comprises elements of a programming language.

22. (Previously presented) A processor, configured in accordance with program code comprising at least one program source code module of a plurality of program source code modules, for translating between high level code and instructions for a target processor, said at least one program source code module being in accordance with a characteristic of said target processor and selected from said plurality of program source code modules.

23. (Previously presented) A processor, configured by program code comprising an agglomeration of two or more program source code modules of said plurality of said program source code modules.

24. (Currently amended) A system comprising a first and second processor, said first and second processor configured in accordance with program code comprising at least two program source code modules, wherein the first of said at least two program source code modules is arranged to translate high level code to instructions for said first processor and a second of said at least two program source code modules is arranged to translate high level code to instructions for said second processor.

25. (Canceled)

26. (Canceled)

27. (Canceled)